**Claims:** (original appn. page 277)

The following is a listing of all claims in the application with their status and the text of all active claims:

1-3. (CANCELLED)

4. (NEW) A data read and write method set called discrete bus, for controlling data transfers internal to a mechanical computer, the method comprising the steps of: providing a first parallel bus having multiple physical paths for one way signals, each data transfer having a first action step of sending a single moving particle as a bit position signal transmitted from a sender physical device to a receiver physical device; including in said bus bit positions both data and control types, and so having an aspect that both physical and operational methods of signaling are the same regardless of type, and so simplifying any associated logic; the method further comprising having the data writing portion of the bus encoding each said bit positional signal into two or more states by distinct path position, and defining the radix range of the data writing portion of the multiple state bit as being the native machine word data range, and herein using the term range on that basis for data reading and writing, such as having ten states encoded for a decimal word in register 700 using a single path encoded bit; further standardizing any apparatus physical bus connectors and conduit positioning according to this discrete bus method; including a minimal useful set of intra-computer elemental data transfer bus functions of interchangeable reading and writing between discrete bus elements herein defined, and a physical device, with reading being a

bus control command bit, called a read sync, sent by bus to said receiver device and writing being a bus multiple valued bit sent by bus to said receiver device; and further providing a reading response method for said receiving device for an automatic action step of output of said multi-valued data bit to a second bus, wherein said discrete bus elemental method set of reading and writing constitutes a useful computer subsystem data transfer method.

5. (NEW) The data transfer method of claim 4, where general additional control commands are optionally added onto the parallel bus definition, herein called an extended discrete bus, by each having a distinct physical path, and by way of example, including the possible options of: a bus control command to said receiving device to increment the internal data stored in said receiving physical device; a bus control command to said receiving physical device to increment internal word value and then output answer as an automatic action step; a similar bus control command to decrement; and a similar bus control command to decrement and output the data result.

6. (NEW) The data transfer method of claim 5, where an optional additional aspect of an extended discrete bus embodiment has a feature of including physical one for one signal translating bus paths, and an automatic action step of horizontal particle movement across defined bus lanes, whereby the simple, single particle data transfer method has an optional aspect of useful processing of said multi-valued bit positional signal.

7. (NEW) The data transfer method of claim 6, where an additional physical bus control signal path called select is added onto the parallel extended discrete bus definition, herein generically termed a mux-bus, comprising: an additional action step of first sending a select, by said physical sending device, on said additional physical bus control path, for causing a physical receiving device to reset one or more internal de-multiplexing means, as a preparatory action; a subsequent one or more action steps of bus transmission of an extended discrete bus signal from said sending device to said receiving device; and one or more internal receiving device actions of de-multiplexing and special use of said one or more extended discrete bus signals.

8. (NEW) The mux-bus method of claim 7, where said physical receiving device is commutating bus switch 840 for random accessed selections establishing paths of transparent connection from a physical discrete extended bus input bus to one of a multiple of physical output bus ports, and where a nested functional aspect is the recombination of said output ports with a select output for each port, with an apparatus method aspect that has said bus switch create each said select from collated re-use of the switch positioning signal, so that each output port in total is also a mux-bus, the method further comprising: reception and special use of the first said extended discrete bus signal particle for commutator positioning, and then for re-transmission as a new mux-bus select to be physically collated and bundled with the bus output that has been selected, whereas the

combination of said mux-bus method, applied to operating the inputs to a bus switch 840, has a nested aspect in that said bus switch as receiving device from the first bus, then becomes also another physical sending device, originating a full mux-bus to each commutated bus port output, and furthermore the method includes an automatic action of said bus switch 840 re-entry to transparent commutator mode, after said first extended discrete bus signal positions said bus switch.

9. (NEW) The method of claim 7, where said physical receiving device is a sequencing bus switch for sequential access to each physical output bus port in turn, shown in figure 28b, by transmitting a single extended discrete bus signal per port, before an automatic action step of internal positioning to the next bus output port in preparation for a next transmission, and furthermore specifying under this method that said physical sending device takes into account the capacity limits of how many ports there are in the receiving device, said sequencing bus switch.

10. (NEW) An alternate embodiment data transfer method generically called a ones transfer mechanical binary bus having the useful function set of reading and writing, in summary for writing comprising the two action steps of clearing all bits in a physical receiving device, followed by sending and setting any bits that are logical ones, the method further

comprising: providing a first parallel physical bus with a bus sub-section for reading having multiple binary bit weighted paths for sending one way reading signals, and a bus sub-section for writing having similar binary bit weighted paths for sending one way data writing signals, and including a bit clearing signal along with said writing sub-section; providing a physical sender device which sends a parallel word of all bits set for reading, and which for writing sends first said clearing signal to said physical receiving device, followed by a write data bus transmission to said receiving device, wherein said ones transfer bus elemental method set of reading and writing constitutes a useful computer subsystem data transfer method.